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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,904	02/08/2002	Mineo Shimotsusa	03500.016184.	8022

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EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/067,904	SHIMOTSUSA, MINEO	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *8-10,12-14,24-26,28-30 and 39-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,16,17,20,22,23 and 32-36* is/are rejected.

7)☒ Claim(s) *5,11,15,21,27,31,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-7, 16-17, 20, 22-23, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent No. 11-031816 Taizo et al., (Japanese Patent Office ComputerTranslation).

1. Referring to claim 1, a semiconductor device in which a switching element for allowing a current to flow to a load and a circuit for driving the switching element are formed on a common substrate, (Figure 1 #11), wherein said switching element is a first insulated gate transistor, (Figure 1 #14A), which comprises: a first semiconductor region of a second conductive type, (Figure 1 #16), disposed at one main surface of a semiconductor substrate of a first conductive type, (Figure 1 #13); a second semiconductor region of the first conductive type, (Figure 1 #13), disposed within the first semiconductor region, (Figure 1 #16); a first gate electrode, (Figure 1 #14A), disposed on a surface in which a pn junction between the second semiconductor region, (Figure 1 #13), and the first semiconductor region, (Figure 1 #16), terminates, through an insulating film, (Figure 4 examiner's label #100); a first source region of the second conductive type, (Figure 1 #20B), which is disposed on one end portion side of said first gate electrode,

(Figure 1 #14A), within said second semiconductor region, (Figure 1 #13); and a first drain region of the second conductive type, (Figure 1 #20A), which is disposed within said first semiconductor region, (Figure 4 #16); and wherein said circuit for driving said switching element comprises a second insulated gate transistor, (Figure 1 #14C), having a characteristic different from that of said first insulated gate transistor, (Figure 1 #14A).

2. Referring to claim 2, a semiconductor device, wherein said second insulated gate transistor, (Figure 1 #14C), constitutes a level shift circuit that generates a drive voltage applied to said first gate electrode, (Figure 1 #14A).

3. Referring to claim 3, a semiconductor device, wherein a drain region, (Figure 1 #20D), of said second insulated gate transistor, (Figure 1 #14C), includes a low impurity concentration region, (Figure 1 #18E).

4. Referring to claim 4, a semiconductor device, wherein said second insulated gate transistor, (Figure 1 #14C), constitutes a level shift circuit that generates a drive voltage applied to said first gate, (Figure 1 #14A), and a low impurity concentration region, (Figure 1 #18E), is disposed within a drain region, (Figure 1 #20D), of said second insulated gate transistor, (Figure 1 #14C).

5. Referring to claim 6, a semiconductor device, wherein a well potential, (Figure 1 #11), of said second insulated gate transistor, (Figure 1 #14C), is different from both a source, (Figure 1 #20C), potential and a drain potential, (Figure 1 #20D).

6. Referring to claim 7, a semiconductor device, wherein a drain region, (Figure 1 #20D), of said second insulated gate transistor, (Figure 1 #14C), has a low impurity concentration region,

(Figure 1 #18E), that is formed to be shallower than said first semiconductor region, (Figure 1 #16).

7. Referring to claim 16, a semiconductor device, wherein said characteristic is at least one selected from a threshold value, a breakdown voltage and a substrate current, (Figure 1).

8. Referring to claim 17, a semiconductor device in which a switching element for allowing a current to flow to a load and a circuit for driving the switching element are formed on a common substrate, wherein: said switching element is formed of a DMOS transistor, (Figure 1 #14A); and said circuit for driving the switching element includes an MOS transistor, (Figure 1 #14C), having a characteristic different from that of said DMOS transistor, (Figure 1 #14A).

9. Referring to claim 18, a semiconductor device, wherein said MOS transistor, (Figure 1 #14C), is of the same conductive type as that of said DMOS transistor, (Figure 1 #14A).

10. Referring to claim 19, a semiconductor device, wherein a drain region, (Figure 1 #20D), of said MOS transistor, (Figure 1 #14C), includes a low impurity concentration region, (Figure 1 #18E).

11. Referring to claim 20, a semiconductor device, wherein said MOS transistor, (Figure 1 #14C), constitutes a level shift circuit that generates a drive voltage applied to a gate electrode of said DMOS transistor, (Figure 1 #14A), and a low impurity concentration region, (Figure 1 #18E), is disposed within the drain region, (Figure 1 #20D).

12. Referring to claim 22, a semiconductor device, wherein a well potential, (Figure 1 #11), of said MOS transistor, (Figure 1 #14C), is different from both a source potential, (Figure 1 #20C), and a drain potential, (Figure 1 #20D).

13. Referring to claim 23, a semiconductor device, wherein a drain region of said MOS transistor, (Figure 1 #14C), has a low impurity concentration region formed to be shallower than a base region, (Figure 1 #13), that becomes a channel of said DMOS transistor, (Figure 1 #14A).

14. Referring to claim 32, a semiconductor device, wherein said DMOS transistor, (Figure 1 #14A), comprises: a first semiconductor region of a second conductive type, (Figure 1 #16), disposed at one main surface of a semiconductor substrate of a first conductive type, (Figure 1 #11); a second semiconductor region of the first conductive type, (Figure 1 #13), disposed within the first semiconductor region, (Figure 1 #16); a first gate electrode, (Figure 1 #14A), disposed on a surface in which a pn junction between the second semiconductor region, (Figure 1 #13), and the second semiconductor region, (Figure 1 #13), terminates, through an insulating film, (Figure 1 examiner's label 100); a first source region of the second conductive type, (Figure 1 #20B), which is disposed on one end portion side of said first gate electrode, (Figure 1 #14A), within said second semiconductor region, (Figure 1 #13); and a first drain region of the second conductive type, (Figure 1 #20A), disposed within said first semiconductor region, (Figure 1 #20D).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent No. 11-031816 Taizo et al., (Japanese Patent Office ComputerTranslation).

15. Referring to claim 33, a semiconductor device, wherein said second insulated gate transistor, (Figure 1 #14C), has an on resistance that is equal or greater, and an operation breakdown voltage that is 2/3 or lower, as compared with those of said first insulated gate transistor, (Figure 1 #14A) and see ** below.

16. Referring to claim 34, a semiconductor device, wherein said second insulated gate transistor, (Figure 1 #14C), has an on resistance that is equal or grater, and the maximum substrate current in an operation range which is 10 times or higher, as compared with those of said first insulated gate transistor, (Figure 1 #14A) and see ** below.

17. Referring to claim 35, a semiconductor device, wherein said MOS transistor, (Figure 1 #14C), has an on resistance that is equal or greater, and an operation breakdown voltage that is 2/3 or lower, as compared with those of said DMOS transistor, (Figure 1 #14A) and see ** below.

18. Referring to claim 36, a semiconductor device, wherein said MOS transistor, (Figure 1 #14C), has an on resistance that is equal or grater, and the maximum substrate current in an operation range which is 10 times or higher, as compared with those of said DMOS transistor, (Figure 1 #14A) and see ** below.

** Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Allowable Subject Matter

19. Claims 5, 11, 15, 21, 27, 31, and 37-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
July 27, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800